Design Guideline for Microfluidic Device and Component Interfaces (Part 2)

Addressing: chip thicknesses, edge-connectors and further miniaturization

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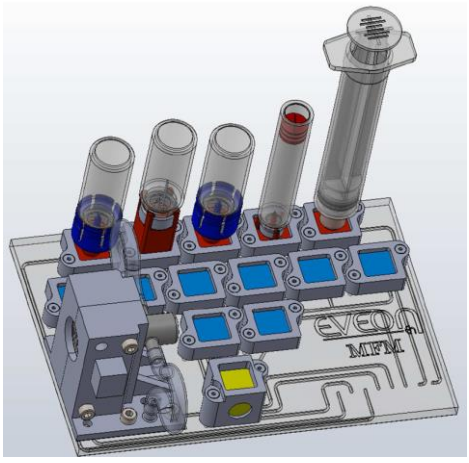

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Contents

2. General introduction

Context

The goal of this document is to facilitate the process of designing new microfluidic sensors, actuators, connectors etc. by providing guidelines for the seamless integration with other microfluidic components and systems. This will overcome the challenge that the process of moving from a research prototype device to a production device takes too long and is too expensive.

Objectives of this paper

This White Paper is an attempt to improve the situation. It is made available for free to developers and researchers around the world who are contemplating the creation of prototype devices containing microfluidics. Its purpose is to present developers a standard by which they will improve the chances of their device will be accepted by the marker / fits to other products.

Positioning of this paper

This paper is “application agnostic” – it is be relevant to people working in: Diagnostics, High Throughput Screening, Sample Preparation, Genomics, PCR, Circulating Tumour Cells, Regenerative Medicine, Flow Chemistry, Environmental, Food and Homeland Security Sensing... and beyond!

This paper is also “materials and production technology agnostic” – we recognise that microfluidic devices can be realised in PDMS, PMMA, COC, Polycarbonate, Glass, Silicon, Metal and Paper as different players specialize in / have a preference for different materials. Furthermore this paper is “manufacturing process agnostic” – recognising again that processes can by company specific. Our vision is that newcomers to the microfluidics market – and companies that want to expand their product portfolio – will look at the relevant guidelines and design according to them. The process to create the products based on these designs will not be described or discussed in this paper. The paper especially addresses topics related to the issue of the microfluidic connections to microfluidic chips or substrates and the integration of microfluidic chips or substrates in components and systems.

Using these design guidelines will be helpful for both user and supplier by ensuring plug and play interconnections.

It is intended that this will be a “living document” updated regularly and the authors are keen on feedback regarding how the document might be improved.

Note: This document does not guarantee IP freedom to operate! There is a complex landscape of patents around microfluidics devices so it is up to you to check whether you need a licence!

The chosen approach concerning the guidelines towards connection/interfacing is to provide the minimum guidelines needed for interoperability, leaving open which materials to be used, what targeted applications and what connections types. We focused on keeping the guidelines simple, understandable by all and implementable by the product manufacturers as well as by the research labs. These guidelines are considered as a first essential step but certainly not an end point.

2 Introduction to this white paper's topics

This white paper is a follow up to our first white paper: Design Guideline for Microfluidic Device and Component Interfaces (part 1), Version 2.0, May 2016, DOI 10.13140/RG.2.1.1698.5206. That paper gave guidelines for:

- axes and reference point for chips,
- microfluidic ports,
- chip formats,
- exclusion zones for clamping or gluing chips,
- dimensions of sensor / Actuator building blocks and
- operational conditions / application classes.

This white paper extends on this and is addressing:

- chip thicknesses,
- edge connectors and
- further miniaturization of chips and connectors.

4 Total chip thicknesses and their tolerances

Often microfluidic components are made by stacking individual chips; for instance channels in one chip covered by another chip which might have other features like sensing, optical access, connections etc. This section deals with total chip stack thicknesses, an important feature for the design of clamped microfluidic connectors, handling in automated equipment etc.

Major considerations for choosing a certain chip thickness include:

- Mechanical strength for automatic or manual manipulation and processing.
- Optical signal attenuation for fluorescence intensity, luminescent intensity, absorbance detection. (For instance for optical access one plate should be as thin as possible.)
- Need for fast heating up / cooling down (for instance for PCR).
- Cost of fabrication.
- Availability of substrates.

The discussion is complicated by the fact that there is no such thing as a standard substrate thickness as shown by the results of a recent survey:

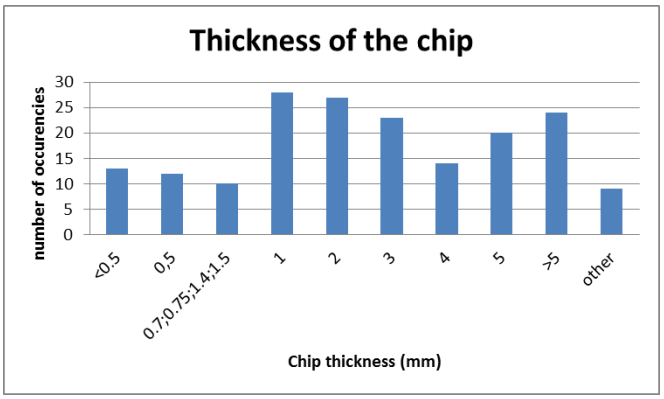

Figure 1: Occurrences of chip thicknesses in microfluidics.

We will therefor approach the topic from two sides:

1) What substrates are available in the market; this argument is especially important for those working with glass.
2) What are the manufacturing constraints; this is for instance important for those that do injection moulding.
3) Constrains from the application; for instance the need for optical access.

Although people often talk about bottom and top plate, in practice this leads to confusion. In this paper we will use the term functional plate, where (most of) the microfluidic are and the cover plate. That does not imply that in the cover plate can't be microfluidic elements.

4.1 Glass wafers

It is advisable to choose from existing standard wafer thicknesses since they are readily available and cheaper since no polishing is required. Moreover, standard wafers have an excellent surface quality, e.g. surface roughness < 1 nm RMS, which in turn has a positive influence in manufacturability and yield. These wafers are available in a number of thicknesses. The company Schott for instance supplies 150 and 200 mm glass wafers with thicknesses between 0.03 mm and 1.1 mm. For D263[1] the standard available thicknesses are:

Table 1: Thicknesses of D263 wafers.

nominal thickness (mm)	thickness tolerance variation in lot (mm)	thickness variation referenced to net width (µm)
0.30	± 0.020	≤ 20
0.40	± 0.020	≤ 20
0.50	± 0.030	≤ 20
0.55	± 0.030	≤ 20
0.70	± 0.050	≤ 30
0.90	± 0.050	≤ 30
1.1	± 0.050	≤ 40

For MEMpax[2] standard available thicknesses are: 0.2, 0.3, 0.4, 0.5, 0.7 mm with similar thickness tolerance and variation as D263[3]. The company Corning supplies glass wafers with thicknesses ranging from 0.4 mm to 1.1 mm, with thickness variation of 1-5%. The thickness standards of silicon wafers are also followed by producers of synthetic quartz wafers, e.g. Asahi Glass Corp and Shin-Etsu.

4.2 Polymer chip thickness

Although other technologies are used, especially for low volume production and R&D, injection moulding is the most common technology to make polymer microfluidic devices. In moulded polymer devices you strive to have all structures in the moulded part. For good mould filling you want the part to be at least 1 mm thick; this thickness is enough for the most often used channel depths (100-300 µm). Increasing thickness has a negative effect of cost. Several suppliers use 1.5 mm as a preferred choice, although microtiterplates are 2 mm thick.

The chips are covered in general with a thin foil. Preferable this foil is commercially available and of the same composition as the functional plate. Typical film thicknesses are between 100 and 250 µm depending on the material. It is important to notice that the structures are usually at the bottom of the moulded part, allowing, if covered by the thin film, a short working distance on an inverted microscope (high NA) as well as a high thermal transmission for e.g. PCR applications.

[1] D 263® T eco is a clear borosilicate glass that has high chemical resistance and is produced by using a SCHOTT-specific down-draw method. It is available in a variety of thicknesses ranging from 0.03 mm to 1.1 mm.
[2] A borosilicate glass that is manufactured with a fire-polished surface.
[3] For instance 0,700mm (+/-0,025)

4.3 Silicon wafers

The often used silicon wafers have standard thicknesses depending on their diameter as shown in the next table.

Table 2: Thicknesses of silicon wafers.

Wafer size	Thickness (mm)
100 mm (usually referred to as "4 inch").	0.525 +/- 0.020
150 mm (usually referred to as "6 inch").	0.675 +/- 0.020
200 mm	0.725 +/- 0.020
300 mm	0.775 +/- 0.020

Silicon wafers of 100, 150 mm and 200 mm are often used to make sensors. 100 mm silicon wafers are slowly disappearing from the market, although still often used for niche applications and R&D.

4.4 Microscope slides and cover slips

Microscope slides are often used by researchers for creating microfluidic devices. There are a number of companies that also use this format. The slides are generally about 1 mm thick (according to the standard the thickness should be between 0.9 and 1.2 mm).

Cover slides[4] are much thinner; several versions are available with thicknesses ranging between 0. 085 and 0.64 mm. See for instance next table.

Table 3: Thickness of Schott D263M cover slides.

Cover slip No.	Thickness (mm)
0	0.085 to 0.13
1	0.13 to 0.16
1.5	0.16 to 0.19
2	0.19 to 0.23
3	0.25 to 0.35
4	0.43 to 0.64

[4] University researchers use coverslip as a cover plate for microfluidic devices, as coverslips are more compatible than glass slides for microscope imaging especially for confocal imaging of cells.

4.5 Most popular chip combinations

As seen above, the variation of thicknesses is large. Not all combinations are practical and after discussions with several users and suppliers we came to the conclusion that the preferred thicknesses are:

- 0.16-0.24 mm (cover slips no 1.5 and 2 fall in this range and also the thinnest glass that is compatible with silicon direct-bonding: 0.2 mm)
- 0.67 - 0.73 mm (the often used 0.7 mm glass wafers and 150/200 mm silicon chips fall in this range)
- 1.5 mm for injection moulded devices
- 2 mm for higher pressure applications

In conclusion we recommend the following combinations for industrial designs:

Table 4: Preferred chip thicknesses and their combinations (thicknesses in mm).

	Functional plate (mm)	Cover plate (mm)	Material	Operational classes[5]	Applications
A	0.7 +/- 0.05	0.2 +/- 0.04	Glass / glass or glass / polymer	PT 2/50; PT 2/75; PT 2/100	General microfluidic applications when optical access or fast heating / cooling is needed.
B	0.7 +/- 0.05	0.7 +/- 0.3[6]	Glass / glass, glass / silicon	PT 2/50; PT 2/75; PT 2/100 PT 7/50; PT 7/75; PT 7/100	General microfluidic applications and microfluidic / silicon sensor combinations.
C	1.05 +/- 0.15	0.2 +/- 0.04	Glass / glass, glass / polymer or polymer / polymer	PT 2/50	R&D applications when optical access is needed, for instance using microscope slides and glass cover slides.
D	1.5 +/- 0.05[7]	0.16 +/- 0.03	Polymer / polymer[8]	PT 2/50; PT 2/75; PT 2/100[9]	General microfluidic applications when optical access is needed.
E	1.5 +/- 0.05[10]	1.5 +/- 0.05	Polymer / polymer	PT 2/50; PT 2/75; PT 2/100.[11]	General microfluidic applications.
F	2 +/- 0.1	2 +/- 0.1	Glass / glass	PT 2/50; PT 2/75; PT 2/100 PT 7/50; PT 7/75; PT 7/100 PT 30/50	High pressure applications.

[5] Operational classes as defined in the first white paper: for instance PT 2/75 means: pressure below 2 bar and temperature between 4 and 75 ˚C.
[6] Be aware, the allowed range for the cover plate is larger than for the functional plate. We have taken a narrower range for the functional plate to ensure enough overlap between chip port and tube opening.
[7] Depending on the design.
[8] The most generally used polymer materials are: COC, PC, PMMA, COP or PS. Not all materials
[9] Depending on the material.
[10] Depending on the design.
[11] Depending on the material:

4 Edge Connectors

Edge connectors are mainly used for glass based microfluidic devices. It is difficult in polymer structured with injection moulding to have channels all the way to the edges of the chip. Polymer chips that are made with other technologies might be used with edge connectors.

Some outcomes from the top connector discussion (see the first white paper) can be used for the edge connector specification: distance to edge (3 mm), port pitch (based on a grid of 1.5 mm) and chip sizes (multiples of 15*15 mm). There are however two additional dimensions to be defined: thickness of the functional plate and thickness of cover plate. Besides that, the specification of the diameter of the port might be different from those of top holes. Only chip to tube connectors will be discussed, the option of an interposer (for fanning out) is not taken into account.

4.1 Reference lines

All distances are given with reference to two lines:

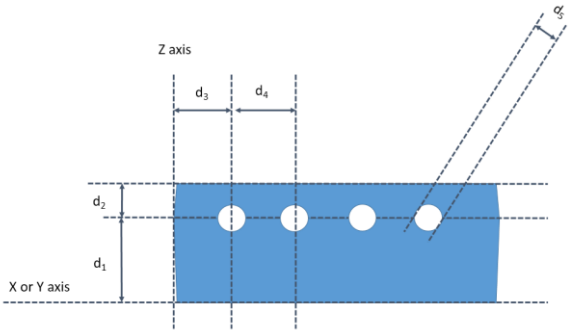

Figure 2: Chip side view: items to be specified for edge connectors.

4.2 Ensuring leak free connections to a chip with tubes

Often used small polymer tubes have an outer diameter of 0.8 mm. In order to have ample room for tolerances and leak free connection of clamped connectors, a minimal stack thickness of 1.4 mm for general use and 2 mm for high pressure applications are recommended by experts[12].

[12] In the future constructions using 0.2 mm coverplates are foreseen.

4.3 Preferred thickness combinations to be used by standard edge connectors

From the discussion above we distinguish the following general cases for edge connectors:

Table 5: Standards for edge connectors († for better alignment of tube to port and better performance, smaller tolerances are generally recommended; ‡ 'socket' seal needed).

	Thickness functional plate (mm)	Thickness cover plate (mm)	Corresponding tubes (mm)[13]	Application	Status
A	0.7 +/-0.05	0.2 +/- 0.04	0.8 or 1.6‡	General applications with optical access	In development
B	0.7 +/-0.05	0.7 +/- 0.3	0.8 or 1.6	General applications; includes glass / silicon	Commercial available
C	1.05 +/- 0.15†	0.2 +/- 0.04	0.8 or 1.6‡	R&D applications; microscope slide with glass cover slides	In development
E	2 +/- 0.1	2 +/- 0.1	0.8 or 1.6	High pressure applications	Commercial available

[13] These are recommended tubesizes, other (smaller) tubes can also be used.

6 Towards further miniaturization of chips and port pitches?

In some cases it might be advisable to use smaller chip; for instance for cost reasons or to minimize dead volume. This chapter shows a route towards smaller chips and their microfluidic connections.

6.1 Port pitches

At this moment the situation is that we based ourselves on a grid of 1.5 mm. A port pitch of 3 mm is state of the art, but information from suppliers gave us confidence that 1.5 mm is realistic. If there is a need to go to even smaller pitches, 0.75 seems to be the obvious choice. Not only this offers a kind of backwards compatibility to the 1.5 grid, it also fits to the potential next step in Microtiterplate miniaturisation where a port pitch of 2.25 mm is foreseen. It must be said that 0.75 mm is not yet proven in technology and application.

6.2 Distance to the edge

Confirming to design constraints from the polymer manufacturers, a distance to the edge of 3 mm is chosen. Glass and silicon manufacturers with their smaller process tolerances are more tolerant to smaller distances. They ensured us that 1.5 mm is certainly possible and 0.75 mm might be realistic.

6.3 Smaller chip sizes

For chip manufacturing processes where the size of the chip is a substantial cost factor (glass processing, but especially silicon processing), the drive towards low cost processing is likely win from any drive to standard chipsizes. The reason is that cost sizes achieved by reducing chipsize will always be substantial more that cost savings due to using standardized chip sizes. Besides, silicon chips are never clamped but always connected to the motherboard by gluing, soldering, using glass frits and other technologies. The exception might be when the chip is packaged and not connected to a motherboard as a bare die. We will therefore discuss not so much chipsizes but package sizes. The package can also be used to fan out the ports. In that case, keeping a distance to the side of 3 mm and a port distance of 3 mm makes sense again, taking into account package technologies. The minimal size of the package will them be determinate by the number of ports.

6.5 Further miniaturization summarized

Table 6: Port pitches and distance to the edge.

Distance to side (mm)	Port pitch (mm)	Technology status
3	3	State of the art, technology proven
3	1.5	State of the art, technology proven
1.5	1.5	Candidate for next step in roadmap, technology feasible
3	0.75	Likely not a standard
1.5	0.75	Likely not a standard
0.75	0.75	Candidate for future step in roadmap, technology challenging

It was decided that it makes sense to let the preferred chipsizes follow the port pitches. That still gives a high number of options. Experts believe that after the following options will be likely choices for the next generation.

Table 7: Preferred options for the next generation small microfluidic chips.

Chip size (mm)	Port pitch (mm)	Distance to the edge (mm)	Maximum number of ports on the short side
15*30	3	3	4
15*15	3	3	4
9 * 15	1.5	3	3
9 * 9	1.5	3	3
6 * 15	1.5	3	1
6 * 9	1.5	3	1

5 And Finally

As said, this White Paper is not a final document; it is just a reflection of the first discussions about microfluidic standards. Experienced engineers will find many other details to specify; organisations working on very lost cost disposables will stress the need for smaller chips and integration. Those interested in shorter times to market and higher reliability will stress the need for industry wide accepted validation test etc. etc.. Therefor we (and hopefully you too) will regard this as a living document. We are interested in your feedback and involvement to improve it!

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To be continued

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